Title

APPARATUS FOR ADJUSTING WOBBLE CLOCK

Background of Invention

1. Field of the Invention

The present invention relates in general to an optical disc drive, and more particularly, to an optical disc drive capable of adjusting the phase of a wobble clock with a frequency divider.

2. Description of the Prior Art

Over the past few years, storage media have rapidly increased in storage capacity due to demand for storing a tremendous amount of information. Of all the various kinds of storage media, optical discs have features of a low-cost, small-size, low-error-rate, long-storage-time, and high-density storage medium and are the most promising dominant storage medium in the future. Generally speaking, optical disc drives are used to read information stored on an optical disc. Examples of optical disc drives are known as compact disc drives (CD-ROM drives) and digital versatile disc drives (DVD-ROM drives) in the prior art. Some optical disc drives have the additional capability of being able to write data onto an optical disc, i.e., CD-R/RW, DVD+R/RW and DVD-R/RW drivers. Optical disc drives are used in music and video playback and are implemented in recording devices and other electronic devices.

In order to effectively manage the information stored on a digital versatile disc, the data storage region of the digital versatile disc is divided into many frames. Data can be stored in these frames according to a memory format. Therefore, while in a writing process for a rewritable digital versatile disc, the DVD drive has to identify the memory format of the rewritable digital versatile disc before the writing process. In order to record the related information concerning the memory frames, there are special addressing structures on the rewritable digital versatile disc to record the

related information. According to the specifications of a recordable or a rewritable digital versatile disc, the related information recorded in the addressing structures is known as the address in pre-groove (ADIP).

It is well-known that the information of the ADIP is recorded in the wobble signal by a phase modulation technique, which means that the information is recorded according to the phase shift of a carrier. Every pair of record areas on an optical disc corresponds to 93 wobble cycles, and 8 wobble cycles of them are utilized to record an ADIP by phase modulation.

Please refer to Figs. 1-3. Figs. 1-3 are diagrams of schematic waveforms of the prior art wobble signals 4a, 4b, and 4c. The wobble signal 4a shown in Fig. 1 comprises 8 wobble cycles W0, W1, W2, W3, W4, W5, W6, and W7, which are utilized to record the information of an ADIP by phase modulation. As is shown in Fig. 1, a phase shift of 180° occurs at the beginning of the first phase-modulated cycle W0 of the wobble signal 4a. In addition, a phase shift of 180° also occurs between the wobble cycle W3 and the wobble cycle W4 of the wobble signal 4a. Consequently, the wobble signal 4a corresponds to an ADIP sync unit. Similarly, the wobble signal 4b shown in Fig. 2 comprises 8 wobble cycles W0, W1, W2, W3, W4, W5, W6, and W7, which are utilized to record the information of an ADIP by phase modulation. As is shown in Fig. 2, a phase shift of 180° occurs at the beginning of the first phase-modulated cycle W0 of the wobble signal 4b. In addition, a phase shift of 180° also occurs between the wobble cycle W0 and the wobble cycle W1 of the wobble signal 4b, and a phase shift of 180° further occurs between the wobble cycle W5 and the wobble cycle W6 of the wobble signal 4b. Consequently, the wobble signal 4b corresponds to an ADIP data unit having a corresponding logic level of 0. Likewise, the wobble signal 4c shown in Fig. 3 comprises 8 wobble cycles W0, W1, W2, W3, W4, W5, W6, and W7, which are utilized to record the information of an ADIP by phase modulation. As is shown in Fig. 3, a phase shift of 180° occurs at the beginning of the first phase-modulated cycle W0 of the wobble signal 4c. In addition, a phase shift of 180° also occurs between the wobble cycle W3 and the wobble cycle W4 of the wobble signal 4c, and a phase shift of 180° further occurs between the wobble

cycle W5 and the wobble cycle W6 of the wobble signal 4c. Consequently, the wobble signal 4c corresponds to an ADIP data unit having a corresponding logic level of 1.

As is described above, the information of an ADIP unit is recorded in the wobble signal by phase modulation, therefore the optical disc drive is required to utilize an ADIP decoder to decode the information of an ADIP unit. Please refer to Fig. 4 in conjunction with Fig. 5. Fig. 4 shows a functional block diagram of a prior art optical disc drive system 10. Fig. 5 is a diagram of schematic waveforms of the wobble signals WBL, WBL', and WBL", and the wobble clock CLK, which are actually the operating clock waveforms related to the optical disc drive system 10 in Fig. 4 with time along the abscissa. The optical disc drive system 10 comprises an optical disc 12 and an optical disc drive 14. The optical disc drive 14 comprises an optical pickup 15, a first band-pass filter 16, a second band-pass filter 18, a wobble clock generator 20, a frequency divider 21, an ADIP decoder 22, and a controller 24.

As is well known in the specifications of a DVD+R disc drive or a DVD+RW disc drive, on the reflecting surface of the optical disc 12, there is a fine spiral track. The fine track is composed of two types of tracks, one being a data track to record data having a value of 0 or 1, and the other being a wobble track to record related addressing information. The data track has an interrupt and discontinuity record mark, and the wobble track has an oscillating shape. The surface of the wobble track protrudes beyond the reflecting surface of the optical disc 12. The data track is located inside a groove formed by the raised wobble track. The length of each record mark varies, and the reflection characteristic of the record mark is different from that of the other reflecting surface of the optical disc.

Consequently, the ADIP is recorded in the wobble track to assist the process of reading or writing data on the data track by the optical pickup 15. Thereby, the optical pickup 15 is able to extract the tracking information carried by the wobble track of the optical disc 12 and generates a wobble signal WBL. The wobble signal WBL is then forwarded to the first band-pass filter 16. The wobble signal WBL' generated by the first band-pass filter 16 based on the wobble signal WBL is forwarded to both the

second band-pass filter 18 and the ADIP decoder 22.

Traditionally, the first band-pass filter 16 is a band-pass filter having a low quality factor (Q-factor), and the second band-pass filter 18 is a band-pass filter having a high quality factor. Because of the first band-pass filter 16 having a low quality factor, the wobble signal WBL' generated by the first band-pass filter 16 based on the wobble signal WBL has the component having a frequency outside the predetermined dominant band suffer from a slight decay as is shown in Fig. 5. On the contrary, because of the second band-pass filter 18 having a high quality factor, the wobble signal WBL" generated by the second band-pass filter 18 based on the wobble signal WBL' has the component having a frequency outside the predetermined dominant band suffer from a significant decay as is shown in Fig. 5.

The wobble signal WBL" is then forwarded to the wobble clock generator 20. The wobble clock generator 20 is utilized to generate a reference clock CLK_REF based on the wobble signal WBL". Traditionally, the frequency of the reference clock CLK_REF is higher than the frequency of the wobble signal WBL". For instance, the frequency of the reference clock CLK_REF is 32 times as high as the frequency of the wobble signal WBL". Accordingly, the frequency divider 21 is required to lower the frequency of the reference clock CLK_REF and generate the wobble clock CLK, for instance the frequency of the wobble clock CLK is 1/32 as high as the frequency of the reference clock CLK_REF. Thereafter, the ADIP decoder 22 is able to decode the ADIP of the wobble signal WBL based on the wobble clock CLK and the wobble signal WBL'. For instance, with the aid of the frequency divider 21, the non-phase-modulated wobble clock CLK is generated through the wobble clock generator 20 based on the phase-modulated wobble signal WBL". Next, the ADIP decoder 22 performs an XOR logic operation over the wobble clock CLK and the wobble signal WBL' to extract the ADIP of the phase-modulated wobble signal WBL. The ADIP generated is then forwarded to the controller 24. Thereafter, the controller 24 is able to perform a reading or writing process on the optical disc 12 based on the ADIP.

As aforementioned, the wobble signal WBL' is generated by the first band-pass filter 16 having a low quality factor based on the wobble signal WBL. Subsequently, the wobble signal WBL" is generated by the second band-pass filter 18 having a high quality factor based on the wobble signal WBL'. Afterward, the reference clock CLK_REF is generated by the wobble clock generator 20 based on the wobble signal WBL". Then, the wobble clock CLK is generated by the frequency divider 21 based on the reference clock CLK_REF. Consequently, a phase delay occurs between the wobble signal WBL' and the wobble signal WBL", and the amount of the phase delay depends on the first band-pass filter 16 and the second band-pass filter 18. Therefore, as the ADIP decoder 22 generates the ADIP by decoding the wobble signal WBL' with the aid of the wobble clock CLK, the phase delay may cause an error operation of the XOR decoding process.

Please refer to Fig. 6. Fig. 6 is a diagram of schematic waveforms of the wobble signal WBL', the ideal wobble clock CLK, the real wobble clock CLK', the ideal processing signal S1, and the real processing signal S2, which are the operating clock waveforms related to the ADIP decoder 22 in Fig. 4 with time along the abscissa. For the sake of clarity, the effects of the first band-pass filter 16 and the noise interference are not under consideration, and the ideal waveform of the wobble signal WBL' is shown in the first waveform of Fig. 6. Then, if the phase delay caused by the second band-pass filter 18 is not under consideration, the ideal waveform of the wobble clock CLK is shown in the second waveform of Fig. 6. However, if the phase delay caused by the second band-pass filter 18 is under consideration, the real waveform of the wobble clock CLK' is shown in the third waveform of Fig. 6. Obviously, there is a phase difference between the real wobble clock CLK' and the ideal wobble clock CLK. In other words, the phase of the real wobble clock CLK' lags the phase of the ideal wobble clock CLK. For instance, as is shown in Fig. 6, the phase difference the real wobble clock CLK' and the ideal wobble clock CLK is 90°. After the ADIP decoder 22 performs an XOR operation over the wobble signal WBL' and the wobble clock, two possible resultant waveforms are shown in Fig. 6. The

fourth waveform of Fig. 6 shows the resultant waveform of the ideal processing signal S1 by an XOR operation over the wobble signal WBL' and the ideal wobble clock CLK. The fifth waveform of Fig. 6 shows the resultant waveform of the real processing signal S2 by an XOR operation over the wobble signal WBL' and the real wobble clock CLK'. Obviously, if the ADIP decoder 22 generates the ADIP by decoding the wobble signal WBL' with the aid of the real wobble clock CLK', the phase delay may cause an error operation of the XOR decoding process as is shown in Fig. 6.

Summary of Invention

It is therefore a primary objective of the claimed invention to provide an optical disc drive capable of adjusting the phase of a wobble clock with a frequency divider to solve the above-mentioned problem of the prior art optical disc drive.

According to a preferred embodiment of the claimed invention, the apparatus capable of adjusting the phase of a wobble clock comprises a phase adjusting circuit for receiving a wobble signal and a wobble clock to generate a phase adjusting value, and a frequency divider connected to the phase adjusting circuit for adjusting the phase of the wobble clock by performing a dividing process on a reference clock according to the phase adjusting value.

According to a preferred embodiment of the claimed invention, the method of adjusting the phase of a wobble clock comprises generating a phase adjusting value based on a wobble signal and a wobble clock, and adjusting the phase of the wobble clock by performing a dividing process on a reference clock according to the adjusting value.

According to the preferred embodiment of the claimed invention, a phase adjusting circuit is utilized to calculate the phase difference between the wobble signal and the wobble clock. Furthermore, the phase adjusting circuit generates a phase adjusting value according to the phase difference. The phase adjusting value is then

forwarded to the frequency divider. When the phase of the wobble signal leads the phase of the wobble clock, the phase adjusting circuit will decrease the phase adjusting value to advance the phase of the wobble clock, which causes the phase difference to reduce. When the phase of the wobble signal lags the phase of the wobble clock, the phase adjusting circuit will increase the phase adjusting value to delay the phase of the wobble clock, which causes the phase difference to reduce.

These and other objectives of the claimed invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

Brief Description of Drawings

Figs. 1-3 are diagrams of schematic waveforms of the prior art wobble signals.

Fig. 4 shows a functional block diagram of a prior art optical disc drive system.

Fig. 5 is a diagram of schematic waveforms of the wobble signals WBL, WBL', and WBL", and the wobble clock CLK related to the optical disc drive system in Fig. 4.

Fig. 6 is a diagram of schematic waveforms of the wobble signal WBL', the ideal wobble clock CLK, the real wobble clock CLK', the ideal processing signal S1, the real processing signal S2 related to the operation the ADIP decoder in Fig. 4.

Fig. 7 shows a functional block diagram of an optical disc drive system according to the claimed invention.

Fig. 8 shows a functional block diagram of the phase adjusting circuit in Fig. 7.

Fig. 9 is a diagram of schematic waveforms of the related signals for the operation of the phase adjusting circuit.

Fig. 10 shows a functional block diagram of the frequency divider in Fig. 7.

Fig. 11 is a diagram of schematic waveforms of the related signals for the operation of the frequency divider.

Detailed Description

Please refer to Fig. 7. Fig. 7 shows a functional block diagram of an optical disc drive system 30 according to one preferred embodiment of the claimed invention. The optical disc drive system 30 comprises an optical disc 32 and an optical disc drive 34. The optical disc drive 34 comprises an optical pickup 36, a first band-pass filter 38, a second band-pass filter 40, a wobble clock generator 40, an ADIP decoder 42, a frequency divider 46, a controller 48, and a phase adjusting circuit 50. Please note that although the frequency divider 46 and the phase adjusting circuit 50 are external to the wobble clock generator 42 in the preferred embodiment, this should not be taken as a limitation. For instance, the frequency divider 46 and the phase adjusting circuit 50 can be integrated into the wobble clock generator 42 according to another preferred embodiment of the claimed invention.

According to the preferred embodiment, the phase adjusting circuit 50 of the optical disc drive 34 is utilized to generate a phase adjusting value PHASEDLY to adjust the phase of the wobble clock generated by the frequency divider 46. Please refer to Fig. 8. Fig. 8 shows a functional block diagram of the phase adjusting circuit in Fig. 7. The phase adjusting circuit 50 comprises a phase-frequency detector (PFD) 52, a counter 54, a clock generator 56, and a decision logic circuit 58. The phase-frequency detector 52 is utilized to compare the phase relationship between the wobble signal WBL' and the wobble clock CLK and generate two corresponding control signals UP and DOWN. For instance, when the wobble signal WBL' switches from a logic level of 0 to a logic level of 1, the phase-frequency detector 52 is triggered to output the control signal UP, which means a rising edge of the wobble signal WBL' is able to trigger the control signal UP. When the wobble clock CLK switches from a logic level of 0 to a logic level of 1, the phase-frequency detector 52 is triggered to output the control signal DOWN, which means a rising edge of the wobble clock CLK is able to trigger the control signal DOWN. For instance, if a rising edge of the wobble signal WBL' occurs at a time T, the phase-frequency detector 52 is triggered to output the control signal UP. Thereafter, if a rising edge of the wobble clock CLK occurs at a time T+dT, the phase-frequency

detector 52 is triggered to output an impulse of the control signal DOWN. Next, the phase-frequency detector 52 will reset the control signals UP and DOWN concurrently. Similarly, if a rising edge of the wobble clock CLK occurs at a time T, the phase-frequency detector 52 is triggered to output the control signal DOWN. Thereafter, if a rising edge of the wobble signal WBL' occurs at a time T+dT, the phase-frequency detector 52 is triggered to output an impulse of the control signal UP. Next, the phase-frequency detector 52 will reset the control signals UP and DOWN concurrently.

The clock generator 56 is utilized to generate a reference clock CLKr and forwards the reference clock CLKr to the counter 54. The counter 54 generates the counting values NUM1 and NUM2 by counting the numbers of cycles of the reference clock CLKr during the corresponding durations of the control signals UP and DOWN. For instance, if the frequency of the reference clock CLKr is Fr and the duration of the triggered control signal UP is Tp1, the corresponding counting value NUM1 is Fr*Tp1. In the same way, if the frequency of the reference clock CLKr is Fr and the duration of the triggered control signal DOWN is Tp2, the corresponding counting value NUM2 is Fr*Tp2. The decision logic circuit 58 calculates a sum based on the counting values NUM1 and NUM2 and determines whether the phase adjusting value PHASEDLY is output to drive the frequency divider 46 to adjust the phase of the wobble clock CLK.

According to the preferred embodiment, the counting value NUM1 is utilized to increase the total sum and the counting value NUM2 is utilized to decrease the sum. For instance, the frequency of the reference clock CLKr generated by the clock generator 56 is 400 times as high as the frequency of the reference clock CLK_REF generated by the wobble clock generator 42, which means one cycle of the reference clock CLK_REF corresponds to 400 cycles of the reference clock CLKr. In other words, the counting value of one cycle of the reference clock

CLK_REF based on the reference clock CLKr is 400. Therefore, when a counting value generated by the counter 54 for the duration corresponding to the phase difference of the wobble clock CLK and wobble signal WBL' is 200, the current phase difference then corresponds to a half cycle of the reference clock CLK_REF.

Since the wobble clock WBL' is generated by the first band-pass filter 38 having a low quality factor, the jitter of the wobble clock WBL' is relatively significant, which means the cycle of the wobble clock WBL' is not quit stable. However, the long-term average of cycles of the wobble clock WBL' is quite stable. As aforementioned, when the phase of the wobble signal WBL' leads the phase of the wobble clock CLK, the counting value NUM1 corresponds to the control signal UP, which means the amount of the phase difference between the wobble signal WBL' and the wobble clock CLK is represented by the counting value NUM1. On the contrary, when the phase of the wobble signal WBL' lags the phase of the wobble clock CLK, the counting value NUM2 corresponds to the control signal DOWN, which means the amount of the phase difference between the wobble signal WBL' and the wobble clock CLK is represented by the counting value NUM2. Under ideal situations, the difference of the sum of the counting values NUM1 and the sum of the counting values NUM2 during a plurality of cycles of the wobble signal WBL' is approximately equal to 0. Furthermore, since the phase of wobble signal WBL" generated by the second band-pass filter 40 is also affected by the second band-pass filter 40. Therefore, according to the preferred embodiment, the decision logic circuit 58 determines whether a phase adjusting value PHASEDLY is generated to drive the frequency divider 46 to correct the phase of the wobble clock CLK based on the difference of the sum of the counting value NUM1 and the sum of the counting value NUM1.

The functional operation of the phase adjusting value PHASEDLY

generated by the decision logic circuit 58 is detailed hereafter. Please refer to Fig. 9 in conjunction with Fig. 8. Fig. 9 is a diagram of schematic waveforms of the related signals for the operation of the phase adjusting circuit 50. The schematic waveform from top to bottom corresponds to the wobble signal WBL', the wobble clock CLK, the control signal UP, the control signal DOWN, the total sum SUM calculated by the decision logic circuit 58 based on the control signals UP and DOWN, the total number CYCLE generated by counting the number of the sums SUM generated by the decision logic circuit 58, and the phase adjusting value PHASEDLY.

For instance, the frequency of the reference clock CLKr generated by the clock generator 56 is 400 times as high as the frequency of the reference clock CLK_REF generated by the wobble clock generator 42, and the phase-frequency detector 52 generates the control signals UP and DOWN according to the rising edges of the wobble signal WBL' and the wobble clock CLK respectively. Therefore, at a time t1 shown in Fig. 9, the rising edge of the wobble signal WBL' drives the phase-frequency detector 52 to generate a control signal UP. At a time t2 shown in Fig. 9, the rising edge of the wobble clock CLK drives the phase-frequency detector 52 to generate a control signal DOWN. After the phase-frequency detector 52 generates an impulse of the control signal DOWN, the phase-frequency detector 52 resets both the control signals UP and DOWN. Then, a counting value NUM1 of 4 is generated by the counter 54 through counting the number of cycles of the reference clock CLKr during the duration of the control signal UP between the times t1 and t2. The decision logic circuit 58 then calculates a sum SUM of 4 and the total number CYCLE of the sums SUM generated is 1. The time duration of the impulse of the control signal DOWN occurs at a time t2 is so short that the current related counting value NUM2 can be neglected. Thereafter, at a time t3 shown in Fig. 9, the rising edge of the wobble clock CLK drives the phase-frequency detector 52 to generate a control signal DOWN. At a time t4 shown in Fig. 9, the rising edge of

the wobble clock CLK drives the phase-frequency detector 52 to generate a control signal UP. After the phase-frequency detector 52 generates an impulse of the control signal UP, the phase-frequency detector 52 resets both the control signals UP and DOWN. Then, a counting value NUM2 of 3 is generated by the counter 54 through counting the number of cycles of the reference clock CLKr during the duration of the control signal DOWN between the times t3 and t4. The decision logic circuit 58 then calculates a sum SUM of 1, i.e. 4 minus 3, and the total number CYCLE of the sums SUM generated is 2. The time duration of the impulse of the control signal UP occurs at a time t4 is so short that the current related counting value NUM1 can be neglected. Similarly, at a time t5 shown in Fig. 9, the rising edge of the wobble signal WBL' drives the phase-frequency detector 52 to generate a control signal UP. At a time t6 shown in Fig. 9, the rising edge of the wobble clock CLK drives the phase-frequency detector 52 to generate a control signal DOWN. After the phase-frequency detector 52 generates an impulse of the control signal DOWN, the phase-frequency detector 52 resets both the control signals UP and DOWN. Then, a counting value NUM1 of 1 is generated by the counter 54 through counting the number of cycles of the reference clock CLKr during the duration of the control signal UP between the times t5 and t6. The decision logic circuit 58 then calculates a sum SUM of 2, i.e. 1 plus 1, and the total number CYCLE of the sums SUM generated is 3. The time duration of the impulse of the control signal DOWN occurs at a time t6 is so short that the current related counting value NUM2 can be neglected. Thereafter, at a time t7 shown in Fig. 9, the rising edge of the wobble signal WBL' drives the phase-frequency detector 52 to generate a control signal UP. At a time t8 shown in Fig. 9, the rising edge of the wobble clock CLK drives the phase-frequency detector 52 to generate a control signal DOWN. After the phase-frequency detector 52 generates an impulse of the control signal DOWN, the phase-frequency detector 52 resets both the control signals UP and DOWN. Then, a counting value NUM1 of 5 is generated

by the counter 54 through counting the number of cycles of the reference clock CLKr during the duration of the control signal UP between the times t7 and t8. The decision logic circuit 58 then calculates a sum SUM of 7, i.e. 2 plus 5, and the total number CYCLE of the sums SUM generated is 4. The time duration of the impulse of the control signal DOWN occurs at a time t8 is so short that the current related counting value NUM2 can be neglected. The above-mentioned procedure proceeds thereafter as is shown in Fig. 9.

According to the preferred embodiment, the decision logic circuit 58 determines whether a phase adjusting value PHASEDLY is generated to drive the frequency divider 46 to correct the phase of the wobble clock CLK based on the result of the phase comparison between the wobble signal WBL' and the wobble clock CLK in a predetermined number of cycles, which is 400 in the current example.

For instance, there are 400 calculations needed for calculating the sum SUM with the decision logic circuit 58 at the time t14. As aforementioned, the duration of the phase difference of the wobble signal WBL' and the wobble clock CLK is evaluated by counting the corresponding number of cycles of the reference clock CLKr through the counter 54. In other words, if a counting value generated by the counter 54 for the duration corresponding to the phase difference of the wobble clock CLK and wobble signal WBL' is 200, the current phase difference then corresponds to a half cycle of the reference clock CLK_REF.

Therefore, if the sum SUM falls into the range between -200 and +200 at the time t14, the corresponding phase difference of the wobble signal WBL' and the wobble clock CLK is less than a half cycle of the reference clock CLK_REF. Under such circumstance, the decision logic circuit 58 is not going to drive the frequency divider 46 to advance or delay a cycle of the reference clock CLK_REF to output the wobble

clock CLK, which means the phase of the wobble clock CLK is held unchanged. That is to say, if the wobble signal WBL' leads the wobble clock CLK by a quarter of a cycle of the reference clock CLK_REF and the decision logic circuit 58 drives the frequency divider 46 to advance the phase of the wobble clock CLK by a cycle of the reference clock CLK_REF, then the phase of the wobble signal WBL' turns out to lag the phase of the wobble clock CLK by three quarters of a cycle of the reference clock CLK_REF, which means the phase difference between the wobble signal WBL' and the wobble clock CLK becomes larger. Consequently, only when the phase difference between the wobble signal WBL' and the wobble clock CLK is less than a half cycle of the reference clock CLK_REF, will the decision logic circuit 58 drive the frequency divider 46 to advance or delay the phase of the wobble clock CLK by a cycle of the reference clock CLK_REF for reducing the phase difference between the wobble signal WBL' and the wobble clock CLK.

As is shown in Fig. 9, a sum SUM of 280 is generated by performing 400 calculations for calculating the sum SUM with the decision logic circuit 58 at the time t14. The sum SUM of 280 is larger than 200, which means that the total duration of the control signal UP is longer than the total duration of the control signal DOWN between the times t1 and t14. In other words, the phase of the wobble clock CLK lags the phase of the wobble signal WBL' in long term average, and the corresponding duration of the phase difference is larger than a half cycle of the reference clock CLK_REF. Therefore, the decision logic circuit 58 drives the frequency divider 46 to advance the phase of the wobble clock CLK by a cycle of the reference clock CLK_REF. Thereafter, the phase difference between the wobble signal WBL' and the wobble clock CLK is reduced to be less than a half cycle of the reference clock CLK_REF. On the contrary, if the value of the sum SUM is less than -200 at the time t14, then the total duration of the control signal UP is shorter than the total duration of the control signal DOWN between the times t1 and

t14. In other words, the phase of the wobble clock CLK leads the phase of the wobble signal WBL' in long term average, and the corresponding duration of the phase difference is larger than a half cycle of the reference clock CLK_REF. Therefore, the decision logic circuit 58 drives the frequency divider 46 to delay the phase of the wobble clock CLK by a cycle of the reference clock CLK_REF. Thereafter, the phase difference between the wobble signal WBL' and the wobble clock CLK is reduced to be less than a half cycle of the reference clock CLK_REF.

According to the preferred embodiment, the decision logic circuit 58 generates a phase adjusting value PHASEDLY and forwards the phase adjusting value PHASEDLY to the frequency divider 46 to adjust the phase of the wobble clock CLK. After performing a predetermined number of counting calculations needed for calculating the sum SUM with the decision logic circuit 58, the decision logic circuit 58 is going to adjust the phase adjusting value PHASEDLY according to the value of the sum SUM. For instance, if the frequency of the reference clock CLKr is N times as high as the frequency of the reference clock CLK_REF and the sum SUM falls into the range between -0.5*N and +0.5*N, then the decision logic circuit 58 holds the phase adjusting value PHASEDLY, which means the phase of the wobble clock should be held unchanged. If the sum SUM is larger than +0.5*N, then the decision logic circuit 58 decreases the phase adjusting value PHASEDLY by 1, which means the phase of the wobble clock should be delayed. If the sum SUM is less than -0.5*N, then the decision logic circuit 58 increases the phase adjusting value PHASEDLY by 1, which means the phase of the wobble clock should be advanced. Thereafter, the frequency divider 46 adjusts the phase of the wobble clock CLK according to the phase adjusting value PHASEDLY. The operation of the frequency divider 46 is detailed hereafter.

Please refer to Fig. 10. Fig. 10 shows a functional block diagram of the

frequency divider 46 in Fig. 7. The frequency divider 46 comprises a counter 60, a register 62, a pulse generator 64, a comparator 66, a D flip-flop 68, and an inverter 70. A counting value COUNT is generated by the counter 60 based on the reference clock CLK_REF and is forwarded to the comparator 66. For instance, the rising or falling edge of each cycle of the reference clock CLK_REF is able to trigger the counter 60 to increase the counting value COUNT. Furthermore, as the counting value COUNT is added to a predetermined critical value, the counter 60 will reset the counting value COUNT to an initial value, and the counting value COUNT accumulates again. According to the preferred embodiment, if the frequency divider 46 generates a wobble clock having a frequency equal to 1/(2n) of the frequency of the reference clock CLK_REF, then the counter 60 will reset the counting value COUNT to an initial value when there are n times of accumulating operation performed by the counter 60.

The register 62 is utilized to store the phase adjusting value PHASEDLY and forwards the phase adjusting value PHASEDLY to the comparator 66. The comparator 66 compares the counting value with the phase adjusting value PHASEDLY and determines whether the counting value is equal to the phase adjusting value PHASEDLY. If the counting value is equal to the phase adjusting value PHASEDLY, the comparator 66 will output an enable signal EN to drive the pulse generator 64 to generate an impulse PULSE. The impulse PULSE is then input to the input terminal C of the D flip-flop 68. The D flip-flop 68 can be triggered by a rising or falling edge of the input signal. If the D flip-flop 68 is triggered by a rising edge of the input signal, then the D flip-flop 68 will transfer the data at the input terminal D to the data output terminal Q at the rising edge of the impulse PULSE. Similarly, if the D flip-flop 68 is triggered by a falling edge of the input signal, then the D flip-flop 68 will transfer the data at the input terminal D to the data output terminal Q at the falling edge of the impulse PULSE. Furthermore, the output data at the output terminal Q is fed back to the input terminal D through an inverter 70. In other words, the logic level of the data at the output terminal Q is different from the logic level of the data at the input terminal D. For instance, if the data at the input terminal D holds a logic level of 1, then the data at the output terminal Q holds a logic level of 0. When the D flip-flop 68

is triggered by an input impulse PULSE, the logic level of the data at the output terminal Q becomes 1, and the logic level of the data at the input terminal D becomes 0 due to the operation of the inverter 70. Similarly, When the D flip-flop 68 is triggered by another input impulse PULSE, the logic level of the data at the output terminal Q becomes 0, and the logic level of the data at the input terminal D becomes 1 due to the operation of the inverter 70. Based on the above description, the logic level of the data at the output terminal Q swaps when the D flip-flop 68 is triggered by an input impulse PULSE generated by the pulse generator 64. The data at the output terminal Q of the D flip-flop 68 is actually the wobble clock CLK.

Please refer to Fig. 11. Fig. 11 is a diagram of schematic waveforms of the related signals for the operation of the frequency divider 46 in Fig. 10. For the sake of clarity, the frequency of the wobble clock CLK generated by the frequency divider 46 is assumed to be 1/32 of the frequency of the reference clock CLK_REF, the counter 60 is assumed to be triggered by the rising edge of the reference clock CLK_REF, and the initial value of the counter 60 is preset to be 0. Consequently, as the counter 60 accumulates the counting value COUNT from the initial value, the counter 60 resets the counting value COUNT after 16 times of accumulating operation as is shown in Fig. 11. For instance, after the rising edge of the reference clock CLK_REF at a time t1 in Fig. 11, the counting value COUNT generated by the counter 60 becomes 15, which means there are 15 times of accumulating operation performed by the counter 60 after a preceded initial value of 0. Consequently, after the rising edge of the reference clock CLK_REF at a time t2 in Fig. 11, the counter 60 will reset the counting value COUNT to be the initial value of 0, and the counting value COUNT starts another counting process based on the rising edge of the reference clock CLK_REF from the initial value. As aforementioned, when the counting value COUNT is equal to the phase adjusting value PHASEDLY, the comparator 66 will output an enable signal EN to drive the pulse generator 64 to generate an impulse PULSE. The impulse PULSE is then input to the input terminal C of the D flip-flop 68. The D flip-flop 68 is then triggered by the rising edge of the impulse PULSE and switches the logic level of the data at the output terminal Q. For example, if the phase adjusting value PHASEDLY is 2, then the logic level of the data at the output terminal

Q switches when the counting value COUNT is equal to 2 at a time t4 or t7, which causes a wobble clock CLKa as is shown in Fig. 11. Similarly, if the phase adjusting value PHASEDLY is 3, then the logic level of the data at the output terminal Q switches when the counting value COUNT is equal to 3 at a time t5 or t8, which causes a wobble clock CLKb as is shown in Fig. 11. Likewise, if the phase adjusting value PHASEDLY is 1, then the logic level of the data at the output terminal Q switches when the counting value COUNT is equal to 1 at a time t3 or t6, which causes a wobble clock CLKc as is shown in Fig. 11.

Obviously, durations of a half cycle of the wobble clocks CLKa, CLKb, and CLKc are all the same, which equal 0.5*T1, and equal the duration of 16 cycles of the reference clock CLK_REF, which equals 16*T2. In other words, the frequencies of the wobble clocks CLKa, CLKb, and CLKc are all the same and equal 1/32 of the frequency of the reference clock CLK_REF. However, because the phase adjusting values PHASEDLY of the wobble clocks CLKa, CLKb, and CLKc are all different, the corresponding phase differences of the wobble clocks CLKa, CLKb, and CLKc are also different. For instance, since the phase adjusting value PHASEDLY of the wobble clocks CLKa is smaller than the phase adjusting value PHASEDLY of the wobble clocks CLKb by a value of 1, the corresponding phase of the wobble clocks CLKa leads the corresponding phase of the wobble clocks CLKb by a duration of a cycle T2 of the reference clock CLK_REF. Similarly, since the phase adjusting value PHASEDLY of the wobble clocks CLKa is larger than the phase adjusting value PHASEDLY of the wobble clocks CLKc by a value of 1, the corresponding phase of the wobble clocks CLKa lags the corresponding phase of the wobble clocks CLKc by a duration of a cycle T2 of the reference clock CLK_REF. Therefore, according to the preferred embodiment, the phase of the wobble clock CLK cab be corrected with the aid of the phase adjusting value PHASEDLY.

As aforementioned, the counter 60 generates counting values COUNT based on the reference clock CLK_REF, and the D flip-flop 68

swaps the logic level of the wobble clock CLK when the counting value COUNT equals the phase adjusting value PHASEDLY. The counting value COUNT generated is recycled within the range of a predetermined value. The predetermined value is actually utilized to define a frequency ratio of the frequency of the reference clock CLK_REF to the frequency of the wobble clock CLK. The phase adjusting value PHASEDLY is utilized to correct the phase of the wobble clock CLK. Therefore, any circuit system having functional operations described above can be integrated into the optical disc drive 34 of the claimed invention as the frequency divider 46.

As is shown in Fig. 9, the value of the sum SUM equals 280 at a time t14. As aforementioned, when the sum SUM is larger than 200, the phase of the wobble clock CLK lags the phase of the wobble signal WBL', and the duration corresponding to the phase difference between the wobble signal WBL' and the wobble clock CLK is larger than a half cycle of the reference clock CLK_REF. Therefore, in order to reduce the phase difference between the wobble signal WBL' and the wobble clock CLK, the decision logic circuit 58 decreases the phase adjusting value PHASEDLY to advance the phase of the wobble clock CLK, which means the following time for the wobble clock CLK to swap the logic level is advanced. For instance, the phase adjusting value PHASEDLY is 2 before the time t14. After the time t14, the phase adjusting value PHASEDLY is decreased to 1. The wobble clock CLKa having a phase adjusting value PHASEDLY of 2 and the wobble clock CLKc having a phase adjusting value PHASEDLY of 1 are both shown in Fig. 11. It is obvious that the phase of the wobble clock CLKc having a phase adjusting value PHASEDLY of 1 leads the wobble clock CLKa having a phase adjusting value PHASEDLY of 2 by a cycle of the reference clock CLK_REF.

On the contrary, when the sum SUM is less than -200 at the time t14, the phase of the wobble clock CLK leads the phase of the wobble signal WBL', and the duration corresponding to the phase difference between the wobble signal WBL' and the wobble clock CLK is larger than a half cycle of the reference clock CLK_REF. Therefore, in order to reduce the

phase difference between the wobble signal WBL' and the wobble clock CLK, the decision logic circuit 58 increases the phase adjusting value PHASEDLY to delay the phase of the wobble clock CLK, which means the following time for the wobble clock CLK to swap the logic level is delayed. For instance, the phase adjusting value PHASEDLY is 2 before the time t14. After the time t14, the phase adjusting value PHASEDLY is increased to 3. The wobble clock CLKa having a phase adjusting value PHASEDLY of 2 and the wobble clock CLKb having a phase adjusting value PHASEDLY of 3 are both shown in Fig. 11. It is obvious that the phase of the wobble clock CLKb having a phase adjusting value PHASEDLY of 3 lags the wobble clock CLKa having a phase adjusting value PHASEDLY of 2 by a cycle of the reference clock CLK_REF.

To sum up, a decreasing of the phase adjusting value PHASEDLY will advance the phase of the wobble clock CLK, and an increasing of the phase adjusting value PHASEDLY will delay the phase of the wobble clock CLK. Therefore, if a corresponding duration of the phase difference between the wobble signal WBL' and the wobble clock CLK is larger than a half cycle of the reference clock CLK_REF, the phase adjusting circuit 50 will increase or decrease the phase adjusting value PHASEDLY and the frequency divider 46 will delay or advance the phase of the wobble clock CLK according to the changing of the phase adjusting value PHASEDLY so as to reduce the phase difference between the wobble signal WBL' and the wobble clock CLK.

According to the embodiment of the claimed invention, please refer to Fig. 7 in conjunction with Fig. 8, a protection signal PROC is generated by the ADIP decoder 44 and is forwarded to the phase-frequency detector 52 of the phase adjusting circuit 50. The protection signal PROC is utilized to stop the phase-frequency detector 52 from outputting the control signals UP and DOWN to the counter 54. The related operation of the protection signal PROC is detailed hereafter.

Please refer to Figs. 1-3. It is well known that the wobble signal WBL comprises a plurality of phase-modulated cycles. After a filtering process is performed by the first band-pass filter 38 on the plurality of phase-modulated cycles of the wobble signal WBL, the corresponding cycles of the wobble signal WBL' become unstable. Under such situation, if the phase-frequency detector 52 compares the unstable cycles of the wobble signal WBL' with the wobble clock CLK, error counting values of NUM1 and NUM2 are generated. The error counting values of NUM1 and NUM2 are forwarded to the decision logic circuit 58, and an error phase adjusting value PHASEDLY is then generated by the decision logic circuit 58, which causes a wrong phase adjusting procedure thereafter. The protection signal PROC is then introduced for the optical disc drive 30 to be capable of avoiding interference generated from any unstable cycle of the wobble signal WBL'.

According to the well-known specifications of the DVD+R optical drive and the DVD+RW optical drive, an ADIP unit corresponds to 93 wobble cycles and 8 wobble cycles of them are utilized to record an ADIP sync unit or an ADIP data unit by phase modulation. The other 85 wobble cycles are not phase modulated to record any information. The 85 non-phase-modulated wobble cycles enclosed in the phase-modulated wobble signal WBL' are then utilized to generate the non-phase-modulated wobble clock CLK. Thereafter, a decoding process performed by the ADIP decoder 44 based on an XOR operation is performed on the non-phase-modulated wobble clock CLK and the phase-modulated wobble signal WBL' to generate an ADIP. Therefore, an ADIP can be generated from the corresponding 8 wobble cycles in an ADIP unit. According to the specifications of the DVD+R optical drive and the DVD+RW optical drive, the subsequent 85 wobble cycles of the wobble signal WBL' should be in phase with the wobble clock CLK. Since an ADIP is decoded with the aid of the wobble clock CLK, the timing for the input of the next first phase-modulated wobble cycle of the wobble signal WBL' can be predicted. Consequently, the timing for the 8 phase-modulated wobble cycles of the wobble signal WBL' to input to the ADIP decoder 44 is preceded by the timing for the

phase-frequency detector 52 to stop outputting the control signals UP and DOWN by the protection signal PROC with a predetermined time interval. As the unstable cycles of the wobble signal WBL' pass away, the protection signal PROC is then reset by the ADIP decoder 44 and the phase-frequency detector 52 is able to output the control signals UP and DOWN again. As a result, with the aid of the protection signal PROC, the phase adjusting circuit 50 is capable of avoiding interference generated from unstable wobble cycles of the wobble signal WBL' and is able to output an accurate phase adjusting value PHASEDLY for the frequency divider 46 to reduce the phase difference between the wobble signal WBL' and the wobble clock CLK.

Compared to the prior art, the optical disc drive of the claimed invention utilizes a phase adjusting circuit to calculate the phase difference between a wobble signal and a wobble clock. Next, a phase adjusting value is generated based on the phase difference and is forwarded to a frequency divider. When the phase of the wobble signal leads the phase of the wobble clock, the phase adjusting circuit will decrease the phase adjusting value to advance the phase of the wobble clock to reduce the phase difference. When the phase of the wobble signal lags the phase of the wobble clock, the phase adjusting circuit will increase the phase adjusting value to delay the phase of the wobble clock to reduce the phase difference. In addition, the ADIP decoder of the claimed invention is able to predict the timing of the next first phase-modulated wobble cycle of the wobble signal and generates a protection signal PROC to stop the phase adjusting circuit from performing the phase adjusting process at a predetermined time before the input of the next first phase-modulated wobble cycle of the wobble signal, which means the optical disc drive of the claimed invention is capable of avoiding interference generated from the phase-modulated wobble cycles of the wobble signal and is able to generate an accurate phase adjusting value PHASEDLY for the frequency divider to reduce the phase difference between the wobble signal and the wobble clock. While the phase adjusting circuit is driving the phase of the wobble clock to be close to the phase of the wobble signal, the ADIP decoder is able to decode the accurate information of an ADIP unit based on the phase-modulated wobble signal with the aid of the wobble clock.

Those skilled in the art will readily observe that numerous modifications and alterations of the device may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.

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